IN THE SPECIFICATION

Please amend the specification as follows.

The paragraph beginning at page 5 is amended as follows:

> The present invention relates to a packaging technology that fabricates build-up layers on an encapsulated microelectronic die and on the encapsulation material that covers the microelectronic die. An exemplary microelectronic package includes a microelectronic die having an active surface and at least one side. An encapsulation material is disposed adjacent the microelectronic die side(s), wherein the encapsulation material includes at least one surface substantially planar to the microelectronic die active surface. A first dielectric material layer may be disposed on at least a portion of the microelectronic die active surface and the encapsulation material surface. At least one conductive trace is then disposed on the first dielectric material layer. The conductive trace(s) is in physical and electrical contact with the microelectronic die active surface. At least one conductive trace extends adjacent the microelectronic die active surface and adjacent the encapsulation material surface.

The paragraph beginning at page 8 is amended as follows:

> A plurality of conductive traces 124 is formed on the first dielectric layer 118, as shown in FIG. 1f, wherein a portion of each of the plurality of conductive traces 124 extends into at least one of said plurality of vias 122 to make physical and electrical contact with the contacts 108. The plurality of conductive traces 124 may be made of any applicable conductive material, such as copper, aluminum, and alloys thereof. As shown in FIG. 1f, at least one conductive trace extends adjacent the microelectronic die active surface 106 and adjacent said encapsulation material surface 110.